Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLEAR**
2. **CLOCK**
3. **A**
4. **B**
5. **C**
6. **D**
7. **ENABLE P**
8. **GND**
9. **LOAD**
10. **ENABLE T**
11. **QD**
12. **QC**
13. **QB**
14. **QA**
15. **RIPPLE CARRY OUTPUT**
16. **VCC**

**.059”**

**14**

**13**

**12**

**11**

**10**

**2 1 16 15**

**3**

**4**

**5**

**6**

**7 8 9**

**MASK**

**REF**

**163**

**LS**

**.060”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND or FLOAT**

**Mask Ref: 163 LS**

**APPROVED BY: DK DIE SIZE .059” X .060” DATE: 8/29/22**

**MFG: NATIONAL THICKNESS .014” P/N: 54LS163A**

**DG 10.1.2**

#### Rev B, 7/1